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A CMOS Ripple Detector for Voltage Regulator Testing

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Abstract This paper presents an RMS based ripple sensor for testing of fully integrated voltage regulators. A DC signal which is proportional to the input ripple amplitude is generated. Final digital pass/fail signal is obtained with a clocked comparator. The sensor can detect a peak-to-peak ripple voltage of up to 50 millivolts on the 1.2 V supply rail and has 220 MHz bandwidth. The sensor is designed using IBM 90 nm CMOS technology and its functionality is verified in Cadence Virtuoso simulation environment.

Keywords Built-in self-test · Supply ripple · Sensor · Voltage regulator · Power management · Testing

1 Introduction

Switching voltage regulators form the main building blocks of power management circuits in any contemporary system on chip (SOC) design due to their high current density and efficiency. However, the presence of output voltage ripple associated with continuous switching is a serious concern. Though this problem can be mitigated through the use of large, off-chip capacitors or by utilizing hybrid systems, it remains a key parameter that should be monitored, especially as supply voltages continue to be reduced [6, 9].

More importantly, there is an emerging trend toward integrating voltage regulators with SOC die/packages to improve efficiency and form factor [2]. This necessitates the use of metal-insulator-metal capacitors and package inductors for signal filtering which suffer from high effective series resistances and DC resistances. Designers are also forced to use small inductor and capacitor values to reduce the resulting footprint. Furthermore, performance of on-chip passive elements is greatly susceptible to process variations. Finally, voltage regulators are required to keep ripple at reasonable levels under a wide range of load conditions due to the development of sophisticated power management units (PMU). As a result, testing of SOCs in terms of supply ripple is becoming more and more important.

Supply ripple can have detrimental effects on the performance of various blocks in an SOC including but not limited to; noise and distortion in analog circuits [6, 9], conversion errors in high performance analog to digital converters [9], and jitter in high speed clock and data recovery circuits [14]. Hence, low supply ripple is crucial for all types of circuits and testing of PMUs in terms of ripple is significant.

"The proportion of test time and diagnosis effort for analog circuitry as a part of total test cost is now much more than the proportion of analog circuit area on entire SOCs" [8]. Measurements done off-chip are time consuming and prone to error due to the inductive and capacitive properties of sensing instruments. Ripple also requires special care in order to

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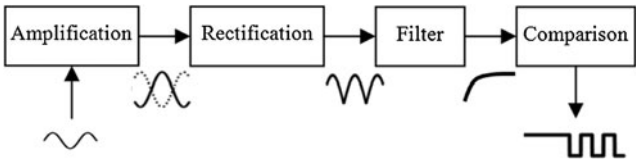

Fig. 1 Block diagram of the ripple detector

avoid coupling of external disturbances. As an analog component, voltage regulators require built-in self-tests (BIST) to increase testing accuracy, accelerate time to market and reduce test costs.

This work proposes a BIST RMS ripple sensor in IBM 90 nm CMOS technology with 1.2 V supply voltage. The RMS sensor is designed to detect 10 to 50 mV peak-to-peak steady state ripple on main supply voltage with a frequency of 200 MHz. The ripple is emulated by a sinusoid superimposed on the supply line. The circuit generates a digital output providing a pass or fail signal based on external DC reference input [12, 13]. The sensor can be integrated on-chip and used during test mode or during normal operation of the SOC due to its low area overhead. The organization of the paper is as follows: Section 2 details the inception of the idea in conjunction with the design specifications. Individual component blocks are presented and elaborated in Section 3 and finally, simulation results and conclusion are present in Sections 4 and 5, respectively.

2 Methodology and Design Specifications

Supply ripple is characterized by low voltage swing and its frequency is directly correlated with the regulator switching frequency. RMS and peak detection are two parameters that

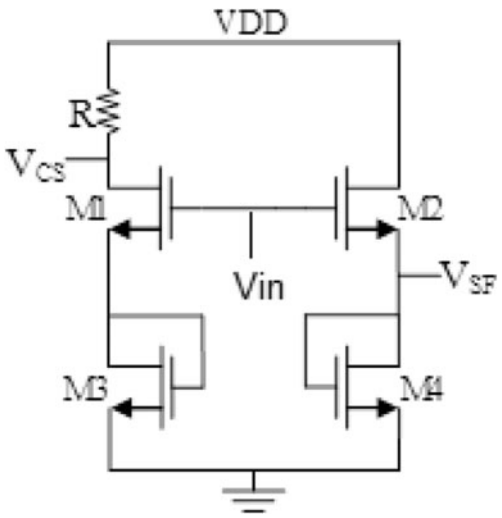

Fig. 2 Common source and source follower stages

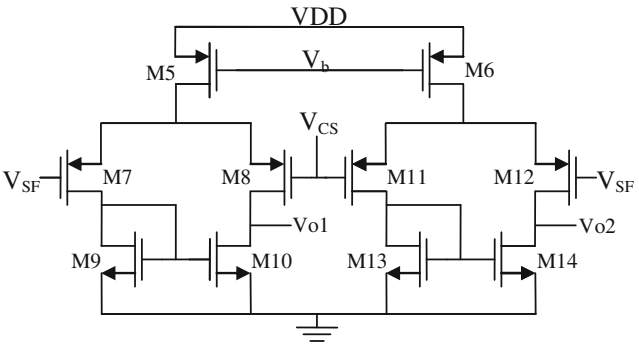

Fig. 3 Differential amplifier stages

can be targeted for amplitude detection. The RMS detection method, which is implemented in this work, has been used in RFICs to test transceiver input and output power levels. The basic idea, given also in Fig. 1, is to amplify, rectify and filter out the ripple signal to obtain a DC output which is proportional to the input amplitude [1, 16]. This method is applied to the ripple on 1.2 V main supply level of IBM 90 nm CMOS technology. To determine the amplifier gain, average ripple levels on integrated voltage regulators are used as reference. Many of the reported ripples range between 14 and 45 mV peak-to-peak [2, 3, 17]. In the light of this data, upper limit for the input ripple is set to 50 mV. A similar search on converter switching frequencies was performed to decide on bandwidth and operating frequency was set to 200 MHz. Low transistor count and total area were prioritized to reduce footprint.

3 Implementation

3.1 Amplifier

Amplification forms the first part of the RMS detector. Due to the low swing and noise resistance of the input

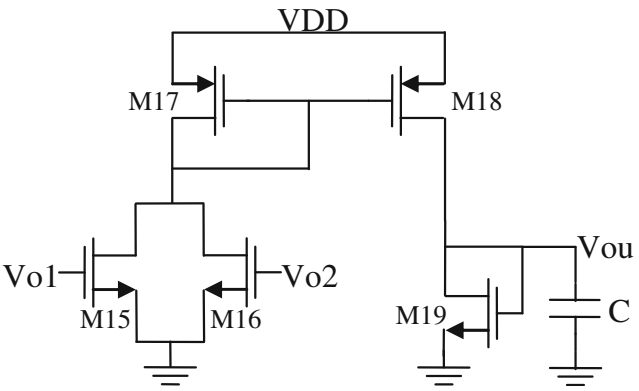

Fig. 4 Full-wave rectifier and filter stages

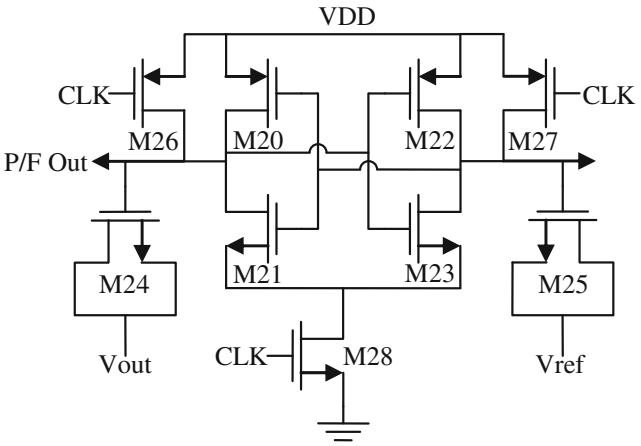

Fig. 5 Clocked comparator

signal, this stage was designed with a differential topology. Figure 2 shows common source and source follower amplifier stages operating with equal gain and output bias levels. They are used to obtain two out of phase inputs for the differential amplifiers [5, 10]. The reason for including the source follower stage is to ensure both signals experience identical latency at 200 MHz, leading to a 180° phase difference. It also shifts the signal bias down to the same level as common source output for proper operation of the differential amplifiers. Note that supply voltage constitutes both the input and VDD of these stages. This made it necessary to use the diode connected transistors M3 and M4 as source degeneration resistors to reduce the overdrive voltages of M1 and M2, forcing them into saturation. The final stages of the amplifier shown in Fig. 3 are the two identical, PMOS driven, current-mirror loaded differential pairs for amplification and to provide a differential output for full-wave rectification [5, 10]. PMOS drivers were chosen for their better noise performance and immunity to body effect when separate wells are used for the two drivers.

In Fig. 2 VCS represents the output of the common source amplifier formed by M1, M3. Its gain is given by:

$$A_{VCS} = \frac{R}{\frac{1}{gm3} + \frac{1}{gm1}} \tag{1}$$

While VSF is the output of the source follower amplifier formed by M2, M4 and the gain is given by:

$$A_{VSF} = \frac{\frac{1}{gm4}}{\frac{1}{gm2} + \frac{1}{gm4}} \tag{2}$$

Most of amplification is done through the differential amplifier, its gain is given by

$$A_V = gm_{8,12}\left(ro_{8,12} \,//\, ro_{10,14}\right) \tag{3}$$

3.2 Full-Wave Rectifier

The second component is comprised of a full-wave rectifier that is driven by the previously described amplifier. Full-wave was preferred over half-wave rectification for several reasons. First, full-wave significantly decreases detection time. In a full-wave rectifier, the frequency of the output signal is twice that of the input and, as a result, the filter at the output stage is expected to settle to a DC level in a shorter period.

Correspondingly, filtering can be achieved by smaller passive elements, which is crucial for low BIST area overhead. The rectifier, which is shown in Fig. 4, consists of a diode connected PMOS (M17) and a driver NMOS pair (M15, M16) operating between weak and strong inversion [7, 16, 18]. The nonlinear behavior of the MOSFETs at this bias condition makes rectification possible. In common mode, all

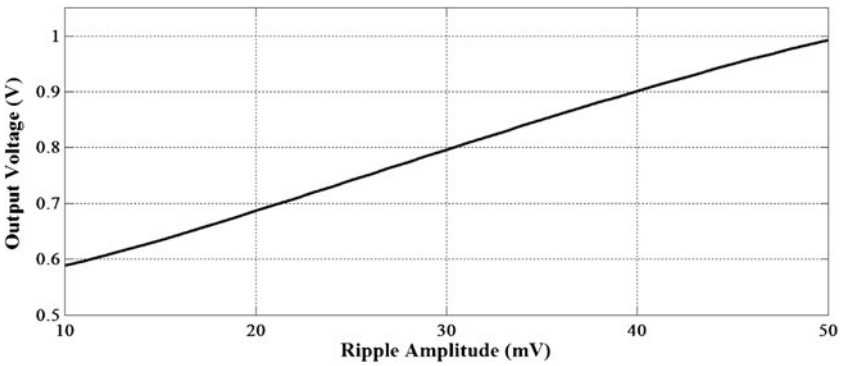

Fig. 6 Input ripple versus filter output

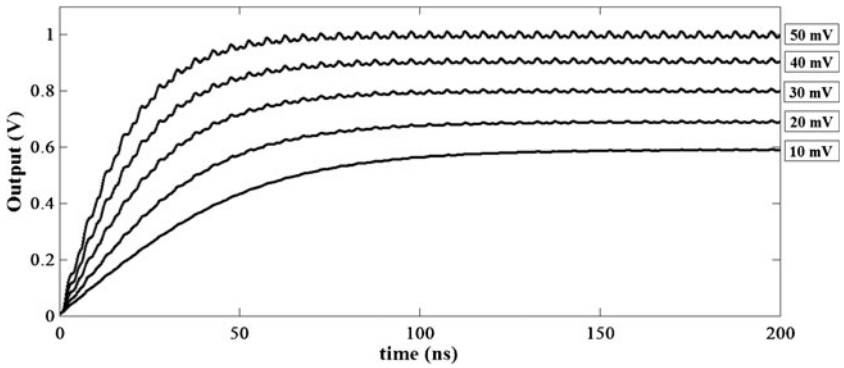

Fig. 7 Response of the ripple detector for varying input ripple amplitudes

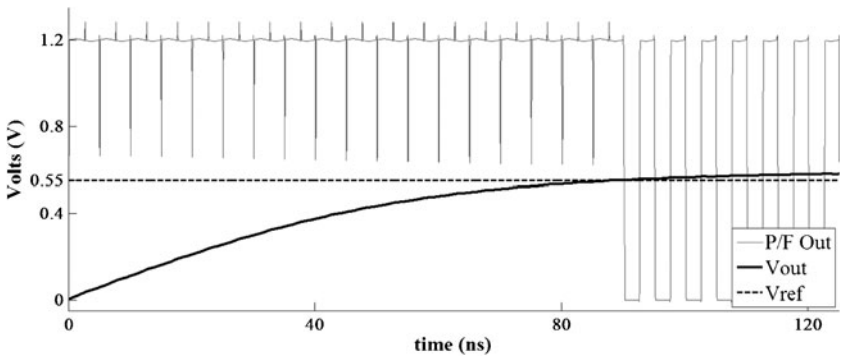

Fig. 8 Filter output, reference and pass/fail signal for 10 mV ripple

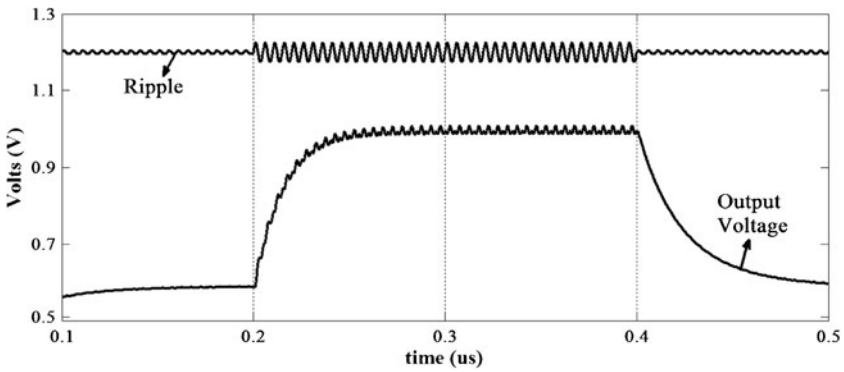

Fig. 9 Transient response of the ripple detector

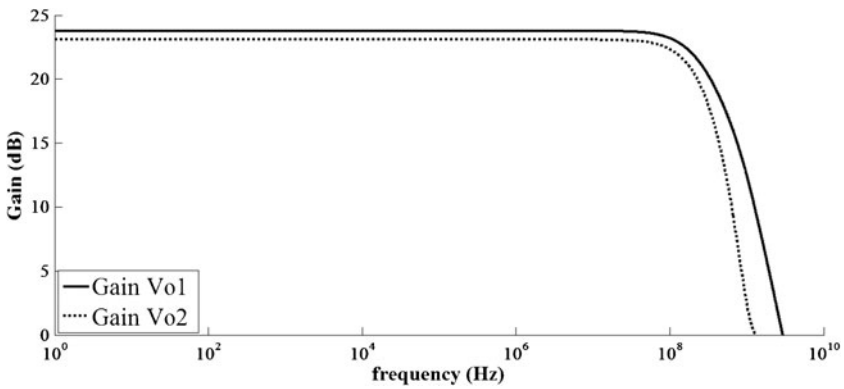

Fig. 10 AC Simulation results of the ripple detector

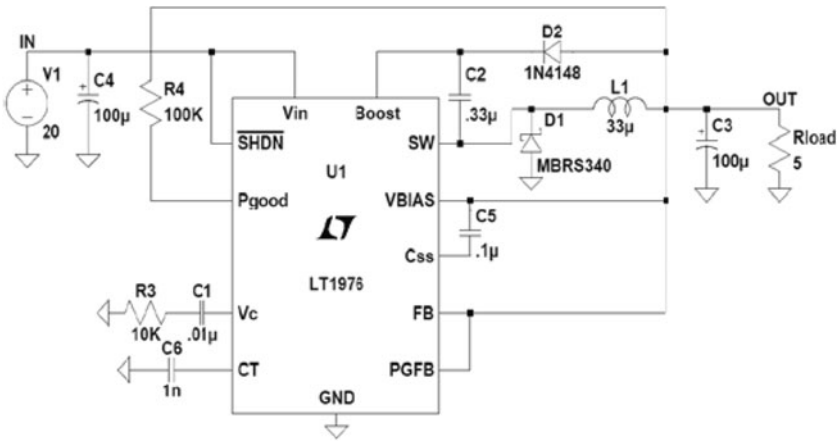

Fig. 11 A step down voltage regulator

the three MOSFETs operate at weak inversion. However, differential inputs (Vo1 and Vo2) force one NMOS (M15 or M16) and the PMOS (M17) to a strong inversion. This creates a rectified current signal passing through M17 and it is mirrored to M18 for filtering.

3.3 Filter

Figure 4 shows the filter stage which includes M18-M19 and a capacitor [16]. Rectified current supplied by M17 is sampled through a mirror transistor, M18. Current division technique is used with low mirroring ratios to yield better filter performance [15]. At the same time, low mirroring ratios decrease the gain of the system whereas high ratios cause higher ripple on the DC output. The ratio is chosen by considering these limitations. Diode connected transistor M19 acts as a resistor and together with the capacitor they create an RC filter. The dimensions of M19 are adjusted to yield higher gate to source voltage, and thus higher DC bias voltage at the output. This is to ensure proper operation of the comparator stage which employs variable MOSFET capacitors where the bias point is crucial. Finally, a smooth DC signal is supplied to the comparator stage.

3.4 Clocked Comparator

The purpose of this stage is to compare the DC output of the filter stage with a reference voltage and generate a pass/fail signal. A clocked, Varicap Threshold Logic (VcTL) topology [4, 11] is used for its simplicity, low transistor count and digital output. These factors were chosen due to their importance in built-in sensor design. The basic design includes two cross-coupled inverters

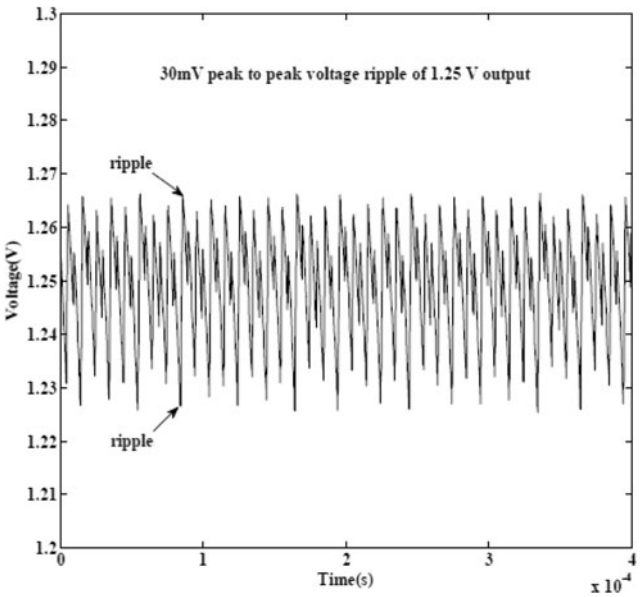

Fig. 12 Voltage ripple of LT1976

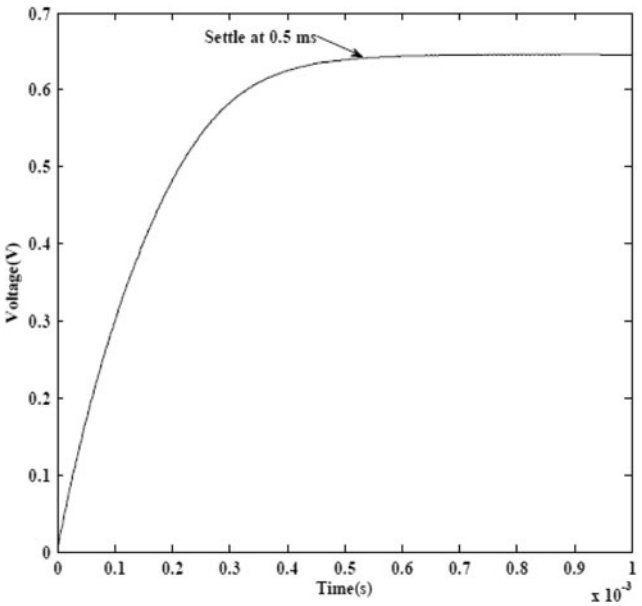

Fig. 13 Output of ripple detector for LT1976

(M20-M23) and two capacitor arrays (M24, M25) as shown in Figs. 5 and 6. The variable capacitor arrays are implemented using NMOS transistors. Operation of the clocked comparator includes two phases, namely pre-charge and evaluation. When CLK is at logic 0, both outputs are pre-charged to VDD through the M26 and M27 transistors. As the CLK signal transitions to logic 1, the outputs start to go to valid states depending on the relationship between input voltage (Vout of the filter) and reference voltage (Vref). This relationship determines the difference between equivalent MOSFET capacitances seen at the output nodes. The node with the higher capacitance discharges slower than the other through M21 or M23. With the positive feedback, output which is denoted by P/F Out is pulled to VDD or ground.

4 Simulation Results and a Test Case

Figure 7 shows a parametric sweep demonstrating the behavior of the sensor at a range of 10 to 50 mV input ripple. After nearly a 100 ns charging period, all outputs settle at DC levels with equal 100 mV separation between adjacent ones. This perfect linearity can be seen more clearly in Fig. 6 which essentially shows input ripple versus DC output for the same range. Figure 8 shows the final digital pass/fail signals coming out of the comparator together with filter outputs and reference signals. After filter outputs exceed reference values, the comparator starts to generate logic 0 at its evaluation phase which represents a fail. Apparently, detection time is dependent on both reference and input ripple levels. Based on the worst case scenario where reference voltage is highest, and input ripple are at lowest level, detection time can be written as 90 ns Figs. 9 and 10.

For a purpose of testing voltage ripple of a voltage regulator, a LT1976 is employed. Some specifications provided by Linear Technology as follows: input voltage range from 3.3 to 60 V, 1.25 A peak switch current, 200 kHz switching frequency, 1.25 V feedback reference voltage. A circuit is built to step down voltage from 12 to 1.25 V, then output voltage ripple will be fed to ripple detector and tested. Figure 11 is the circuit and Fig. 12 illustrates the 30 mVpp ripple of output voltage. Figure 13 shows the DC output of the ripple detector, which is proportional to the 30 mv ripple.

5 Conclusion

A CMOS RMS detector system for on-chip supply ripple testing is proposed. The results demonstrated perfect linearity at the targeted range of 10 to 50 mV peak-to-peak ripple. To show the possibility of sensor in both test and normal operation modes, transient response with changing ripple is given in Fig. 9. It demands a clock and an external DC reference input. Detection time, which is dependent on ripple level and reference, is less than 90 ns. It is also proven that the circuit can operate with high linearity within a 220 MHz bandwidth as shown in Fig. 10. Consequently, the technique proves to be promising, especially in regards to fully integrated voltage regulators at high switching frequencies. For future work, it is targeted to add programmability and measure ripple on multiple voltage domains.

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